SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech I Year II Semester Supplementary Examinations May/June-2024
DIGITAL LOGIC DESIGN
(Common to CSE & CSIT)

Time: 3 Hours   **Max. Marks: 60**

(Answer all Five Units 5 x 12 = 60 Marks)

UNIT-I

1	a	(i)Convert $(0.6875)_{10}$ to binary. (ii) Using 10's complement, subtract 72532 - 3250.	CO1	L1	6M
	b	(i) Draw the graphic symbols and truth tables of the eight digital logic gates. (ii) Write short notes on different digital logic families of digital integrated circuits.	CO1	L2	6M

OR

2	a	Express the following function as a sum of minterms $F(A,B,C,D) = B'D + A'D + BD$	CO1	L4	6M
	b	Express the complement of the following function in sum-of-minterms form: $F(A,B,C,D) = \Sigma(3,5,9,11,15)$	CO1	L4	6M

UNIT-II

3	a	Draw the logic diagram of a parity generator and checker and explain it.	CO2	L3	6M
	b	Draw the multi-level NAND circuit for the following expression: $w(x+y+z) + xyz$	CO2	L3	6M

OR

4	a	Simplify the following Boolean functions, using three-variable maps: (a) $F(x, y,z) = \Sigma(0,2,6,7)$ (b) $F(x, y, z) = \Sigma(0,2,3,4,6)$	CO2	L2	6M
	b	Give three possible ways to express the following Boolean function with eight or fewer literals: $F = B'C'D' + AB'CD' + BC'D + A'BCD$	CO2	L2	6M

UNIT-III

5	a	Brief Combinational circuit and draw the block diagram of combinational circuit.	CO3	L5	6M
	b	Elaborate the analysis procedure of a combinational circuit with a logic diagram.	CO3	L2	6M

OR

6	a	Explain how to implement a Half Adder.	CO3	L5	6M
	b	Construct 4 x 16 decoder with two 3 x 8 decoders	CO3	L6	6M

7	a	Reduce the number of states in the following state table, and tabulate the reduced state table:	CO4	L6	6M

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

	b	What is shift register? Enumerate the types of shift registers. Give few applications of shift registers.	CO4	L1	( )

OR

8	a	Discuss Ring counter and Johnson Counter.	CO4	L6	6M
	b	Explain JK flip flop and show how the JK Flip Flop removes the drawbacks of SR Flip Flop.	CO4	L2	6M

UNIT-V

9	a	Elucidate Memory unit and its types with a neat block diagram.	CO5	L2	6M
	b	Discuss types of Read only Memory in detail.	CO5	L6	6M

OR

10	a	Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.	CO5	L6	6M
	b	Implement the following two Boolean functions with a PLA: $F_1(A, B, C) = \sum(0, 1, 2, 4)$ $F_2(A, B, C) = \sum(0, 5, 6, 7)$	CO5	L2	6M

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